CLAIMS

What is claimed is:

1. An apparatus for evaluating at least one timer in the event of a timeout condition in a system comprising:

first circuitry that generates an indication that certain system conditions have occurred;

clock circuitry, enabled by said indication, that generates a timeout counter enable signal;

a plurality of timer units, coupled to said clock circuitry, wherein an output of each of said plurality of timer units is incremented by individual ones of a plurality of incrementing signals and reset by individual ones of a plurality of monitored signals, wherein said monitored signals are representative of conditions in said system; and

comparison circuitry coupled to said plurality of timer units, such that when an output of at least one of said plurality of timer units reaches a predetermined count, the count of each of said plurality of timer units is stored.

2. The apparatus of claim 1, wherein said first circuitry comprises circuitry indicating that a sequence of events in said system have occurred.

3. The apparatus of claim 2, wherein said first circuitry comprises a state machine responsive to signals present in said system.

4. The apparatus of claim 1, wherein said first circuitry comprises circuitry indicating that a predetermined number of events in said system have occurred.

5. The apparatus of claim 4, wherein said first circuitry comprises a comparison circuit for comparing signals present in said system with a predetermined number.

6. The apparatus of claim 1, wherein said individual ones of said plurality of incrementing signals are synthesized from said timeout counter enable signal either alone or in combination with other signals from said system.

7. The apparatus of claim 1, wherein each of said timer circuits further comprises:

a counter, incremented by one of said incrementing signals and reset by one of said monitored signals;

a latch circuit coupled to the output of said counter; and

a comparison circuit, couple to said counter and to said latch circuit such that the output of said counter is compared to the contents of said latch and loaded into said latch if said output is greater than said contents.

8. The apparatus of claim 1, further comprising a data multiplexer for accessing the stored count of each of said plurality of timer units.

9. A method for evaluating timers or timeout conditions in a system comprising the steps of:

generating an indication that certain system conditions have occurred;

generating a timeout counter enable signal enabled by said indication;

incrementing a plurality of counter circuits by individual ones of a plurality of incrementing signals and resetting said plurality of counter circuits by individual ones of a plurality of monitored signals, wherein said monitored signals are representative of conditions in said system; and

comparing the outputs of said plurality of counter circuits, and when at least one of said plurality of counter circuits reaches a predetermined count, latching the output of each of said plurality of counter circuits.

10. The method of claim 9, wherein said certain system conditions comprise a sequence of events that have occurred in said system.

11. The method of claim 9, wherein said certain system conditions comprise a predetermined number of events that have occurred in said system.

12. The method of claim 9, further comprising synthesizing individual ones of said plurality of incrementing signals from said timeout counter enable signal either alone or in combination with other signals from said system.